



32GT/s Channel Design

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Acknowledgments



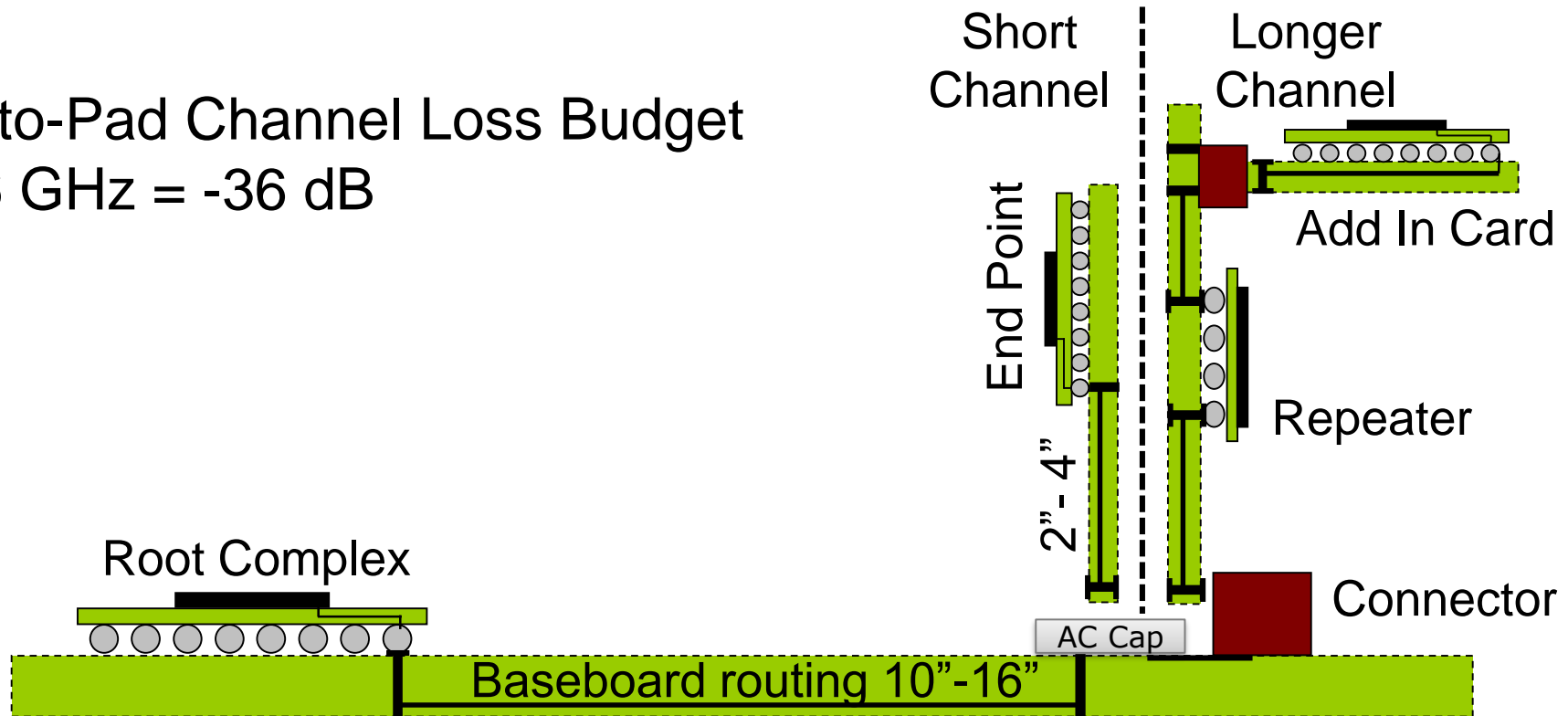
- **Anupriya Sriramulu**
- **Prerana Singaraju**
- **Raul Enriquez**
- **Daniel Froelich**

- **An Example PCIe® Channel Topology**
- **Key Channel Enablers for 32GT/s**
- **Pad-to-Pad Channel Characteristics**
- **Channel Quality Metrics**
- **Impact of Design and Manufacturing Variations**
- **Summary**

A Typical PCIe Channel Topology



Pad-to-Pad Channel Loss Budget
at 16 GHz = -36 dB

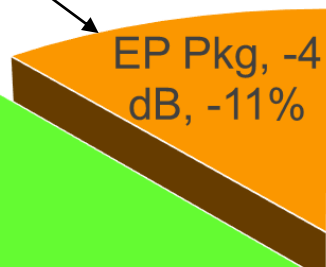


Most server platforms require 10"-16" system channel reach

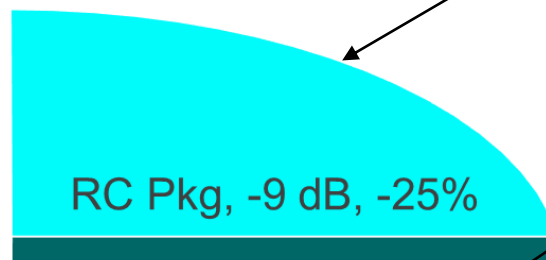
32GT/s Channel Loss Budget



End Point Package



Root Complex Package



Pin-to-Pin Routing: - 19 dB
Vias & Connector: - 4 dB
Up to 19" for 1 dB/in PCB loss

Pin-to-Pin Channel, -23 dB, -64%

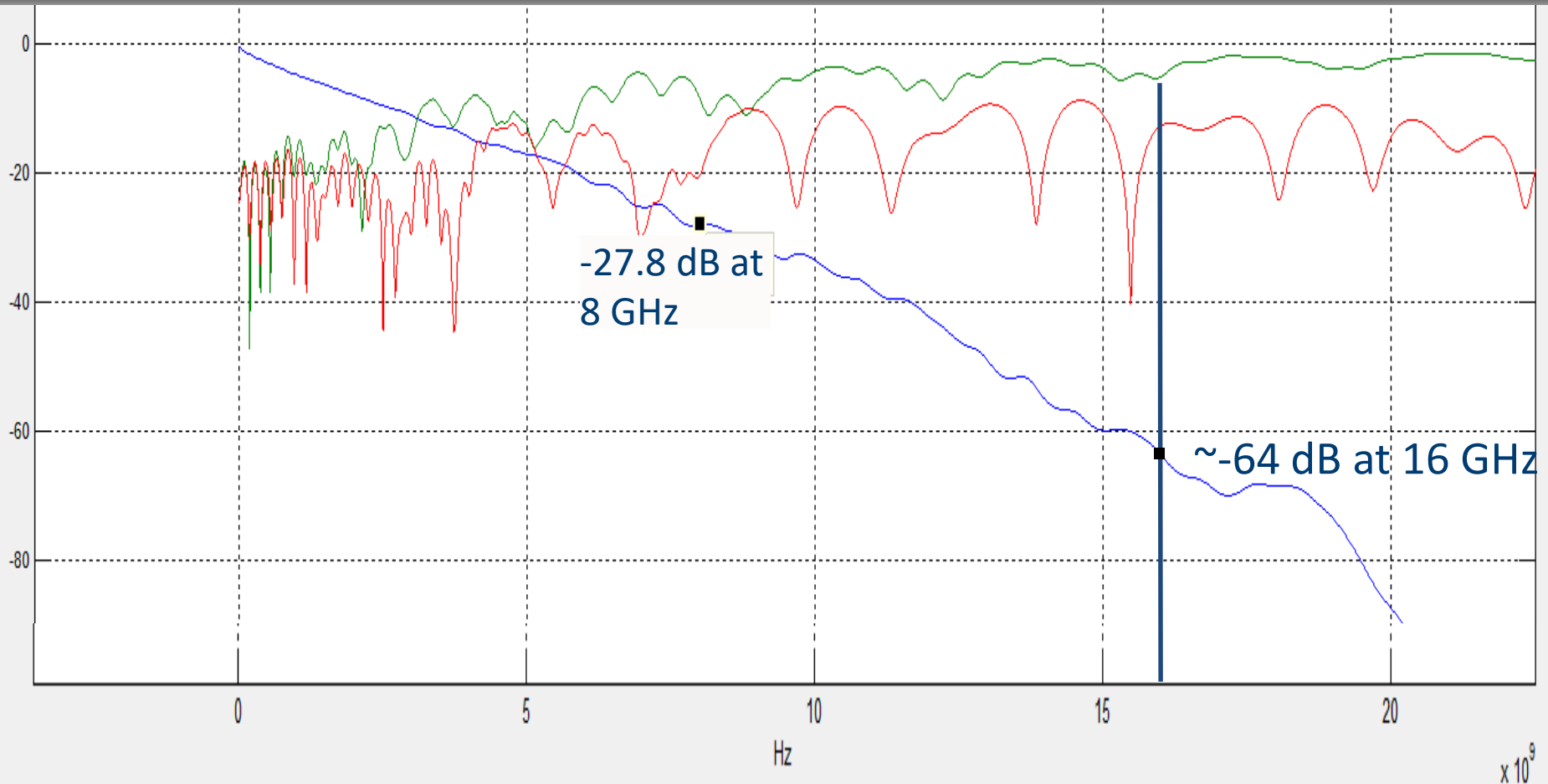
2"-4"

AC Cap

Baseboard routing ~10"-16"

Megtron6-like 1 dB/in PCB Material is needed for most platforms

Typical PCIe 4.0 Pad-to-Pad Loss



Every channel component needs > 2x improvement

32GT/s Channel Assumptions



Root Complex Package-Socket:

Loss ~ -8.5 dB at 16 GHz

Baseboard:

Stripline Routing: 16"

Loss: 1.0 dB/in at 16 GHz (Meg6 like)

Impedance: 85 Ω

Add-in-card:

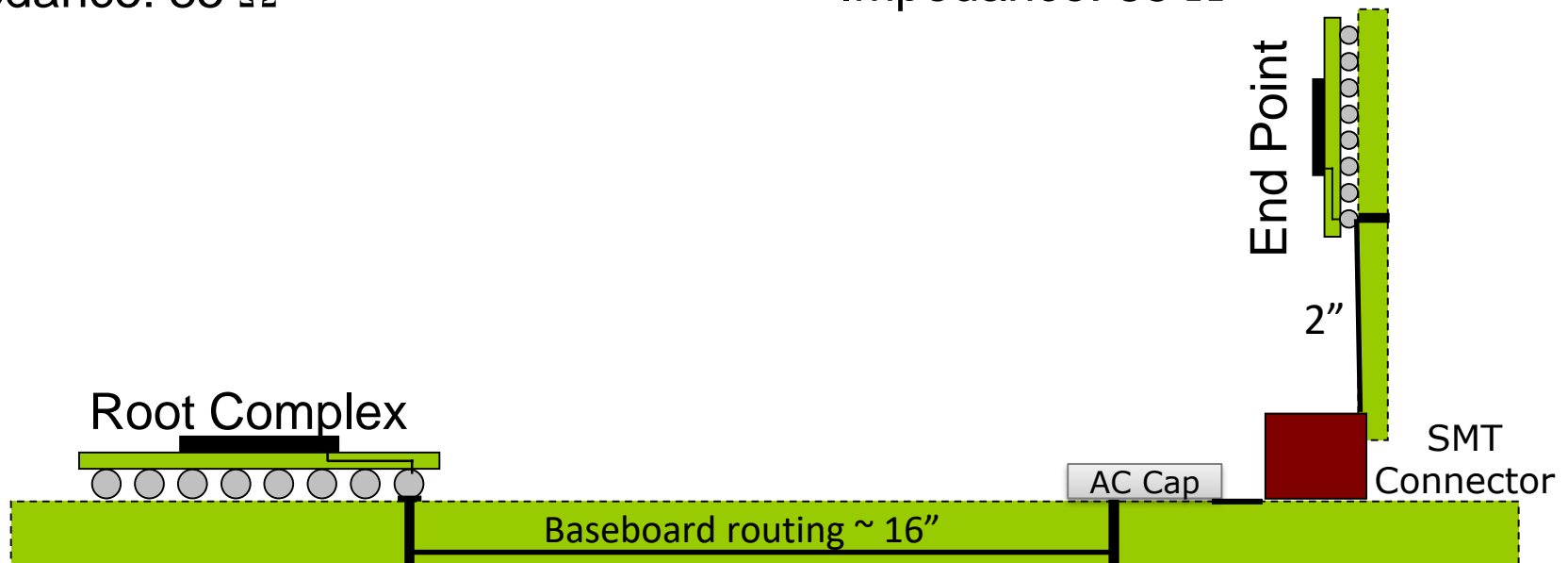
Microstrip Routing: 2"

Loss: 1.58 dB/in at 16 GHz

End Point Package:

Loss ~ -4 dB at 16 GHz

Impedance: 85 Ω



Pad-to-pad channel loss at 16 GHz ~ -32.4 dB

32GT/s Silicon Assumptions



Tx Silicon

Adaptive 3-tap Tx EQ

Tx uncorrelated total jitter = 6.25 ps

Reference clock random jitter w/ system noise = 250 fs

Rx Silicon

Eye mask: Eye height = 10 mV and Eye width = 0.3 UI

Adaptive CTLE (low frequency and high frequency equalization)

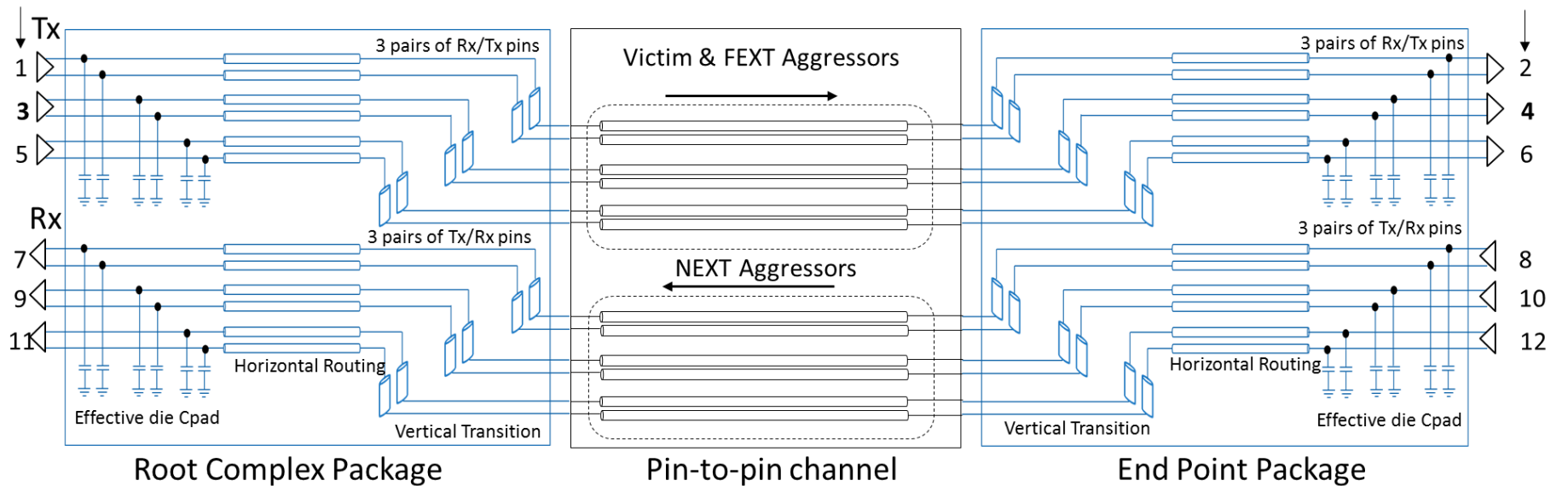
- Transfer function with 4 poles, 2 zeros

3-tap DFE

2x improvement in Si jitter, noise, and equalization compared to 16GT/s design

Simulation Schematic

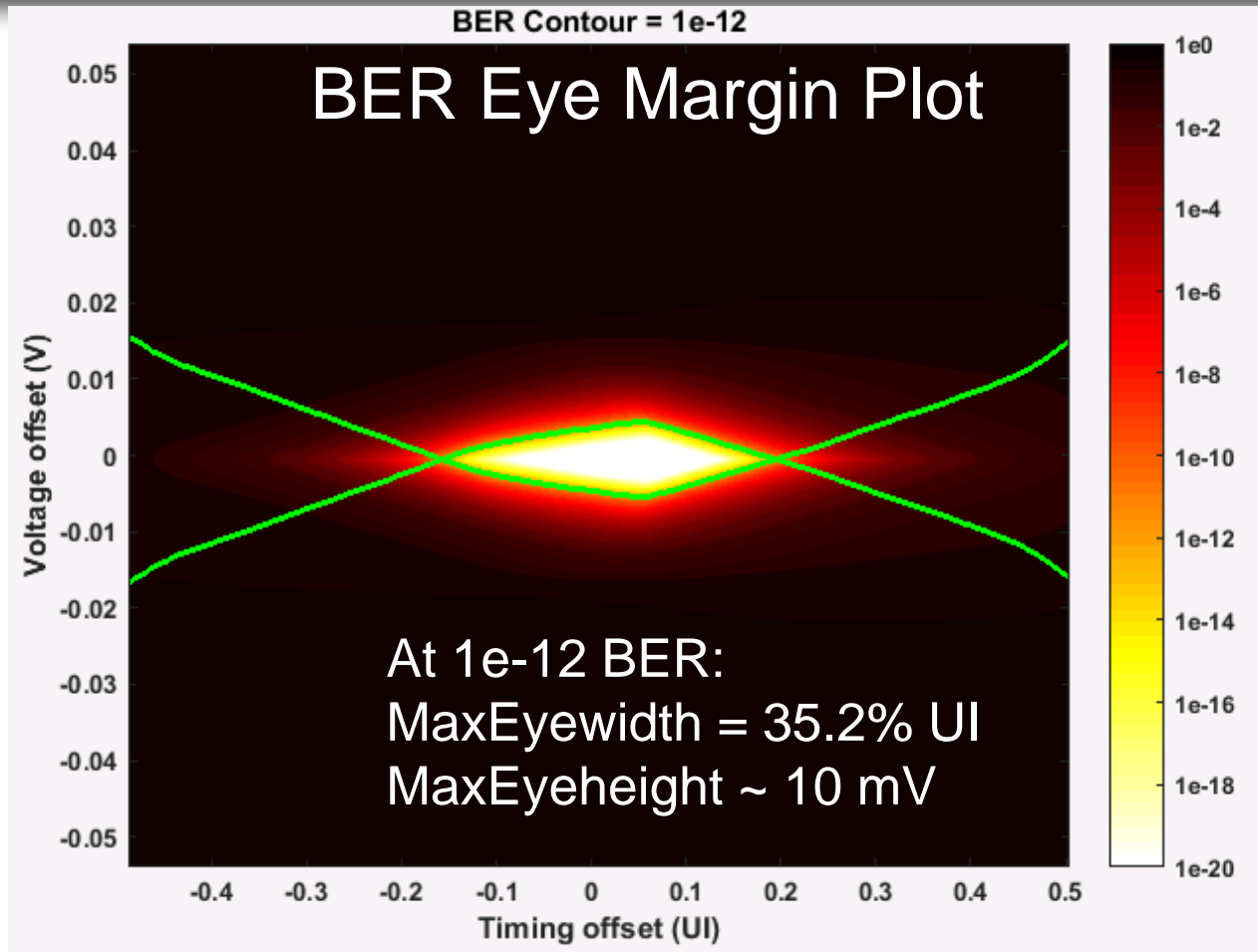
Differential Port#



(via + baseboard routing + via + Cap + baseboard routing + conn + AIC routing)

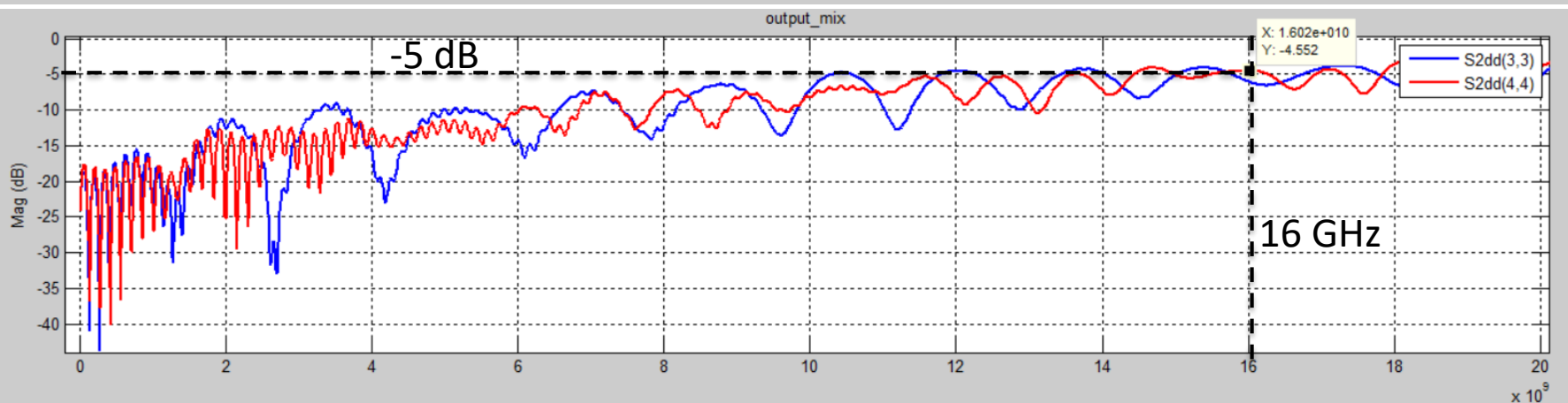
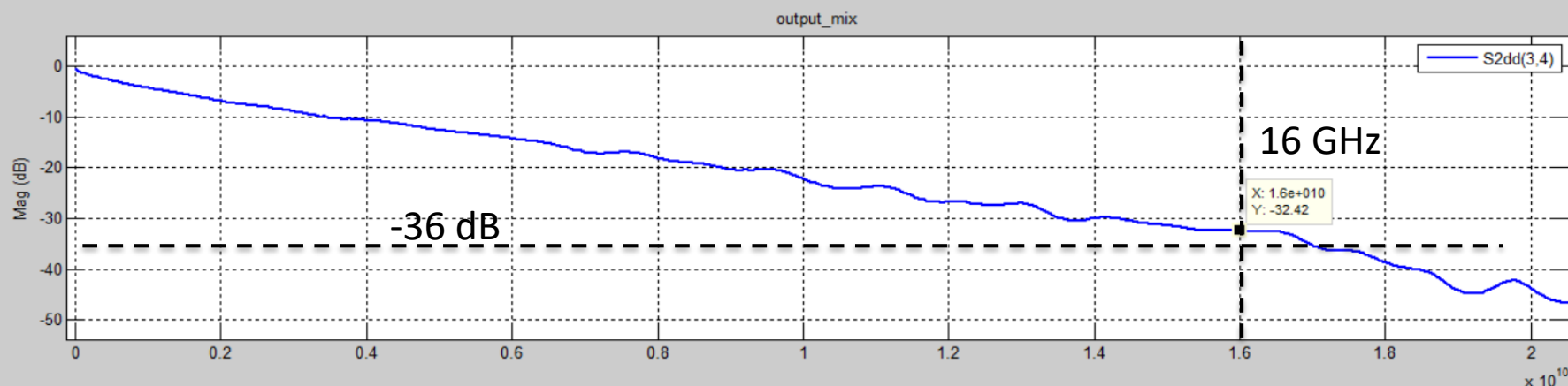
Lane 3->4 is worst-case victim with two Far-end Crosstalk (FEXT) and three Near-end Crosstalk (NEXT) aggressors

Eye Diagram for Example Case



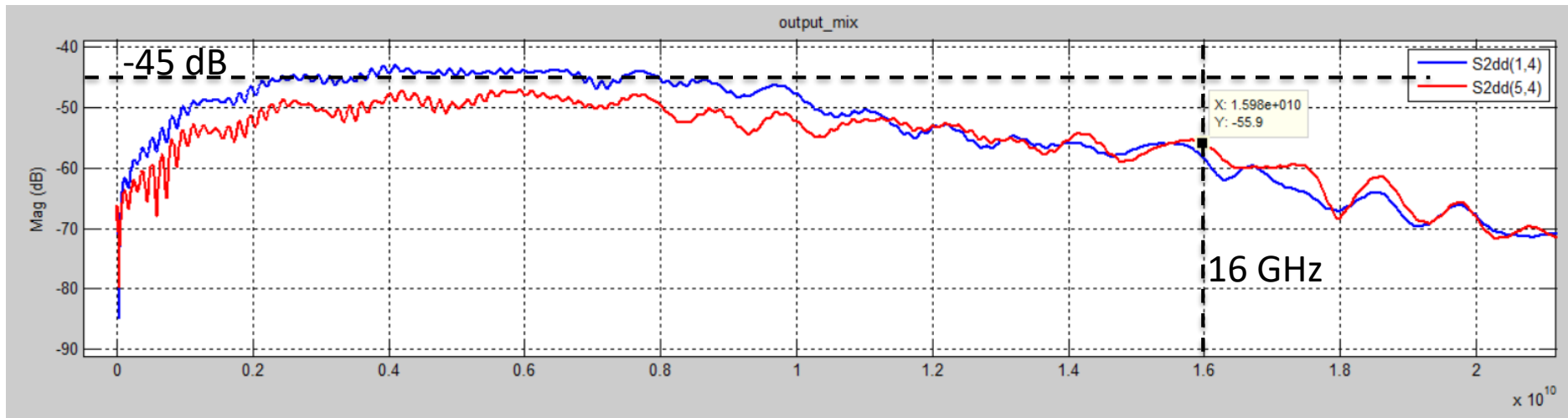
32GT/s is feasible with realistic Si and channel enablers

Pad-to-Pad Channel Insertion and Return Loss



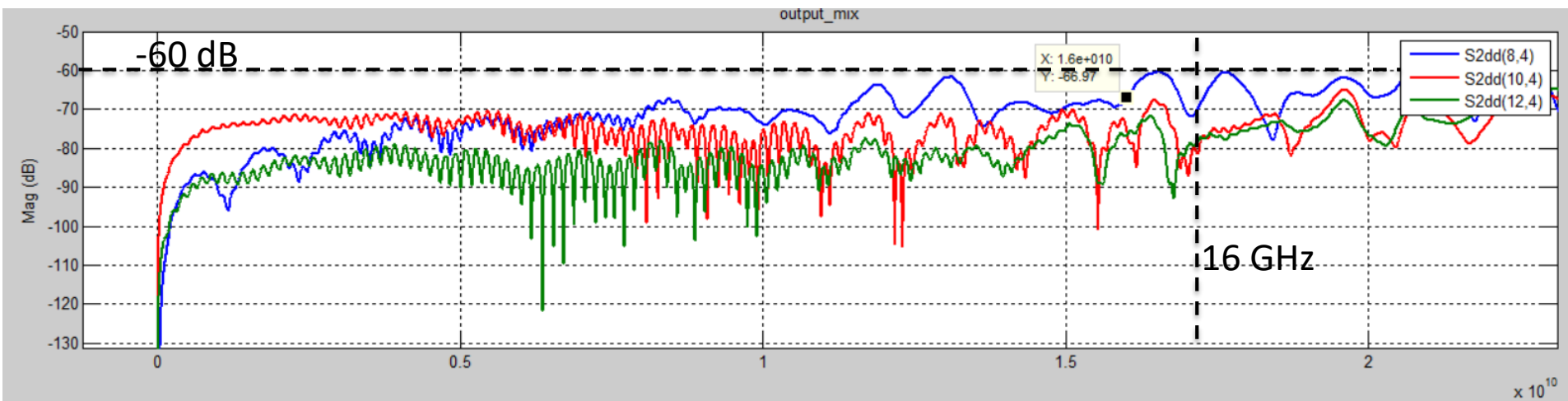
IL < -36 dB at 16 GHz and RL < -5 dB up to 16 GHz

Far-end Crosstalk (FEXT)



Far-end crosstalk is significantly below -40 dB across the frequency spectrum

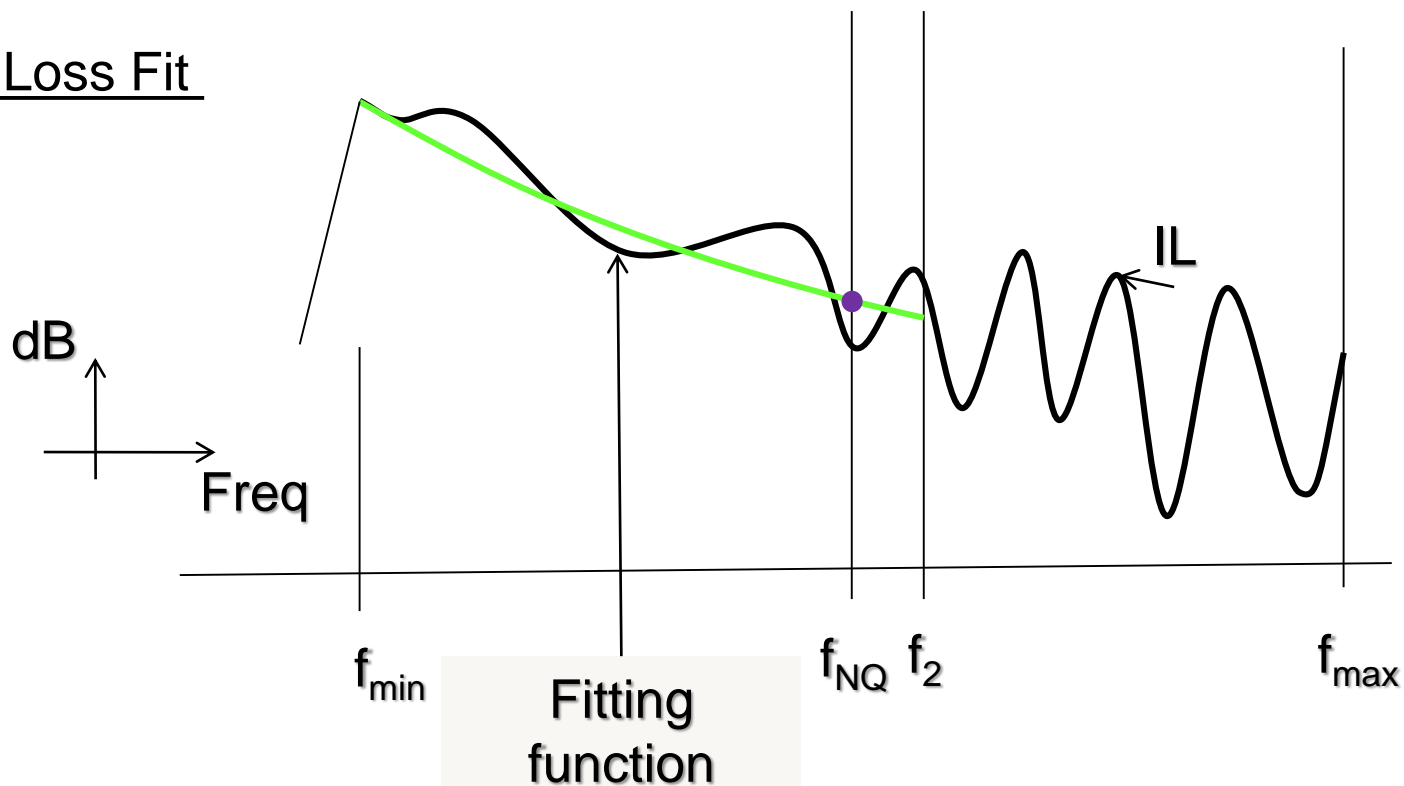
Near-end Crosstalk (NEXT)



Near-end crosstalk is significantly below -60 dB across the frequency spectrum

Channel Quality Metrics

Insertion Loss Fit



$$IL_{fit}(f) = \alpha_0 + \alpha_1 \cdot \sqrt{f} + \alpha_2 \cdot f + \alpha_3 \cdot 10^{\frac{-8 \cdot \sin(\pi \cdot f \cdot UI)^2}{20}} + \alpha_4 \cdot 10^{\frac{-8 \cdot \sin(2\pi \cdot f \cdot UI)^2}{20}}$$

A Healey, "Noise considerations for 40/100GBASE-CR4/10", healey_02_0709.pdf, IEEE P802.3ba 40Gb/s and 100Gb/s Ethernet Task Force, July 2009, San Francisco, CA.

Channel Quality Metrics

$$ILN(f_{ni}) = \left| sdd21(f_{ni}) \right| - 10^{\frac{ILfit(f_{ni})}{20}}$$

$$\sigma_{ILN} = \sqrt{\frac{\sum_n PWF(f_n) \cdot ILN(f_n)^2}{\sum_n PWF(f_n)}}$$

$$\sigma_{xtp} = \sqrt{\frac{\sum_n PWF(f_n) \cdot \sum_x A_x^2 |SDD21xtp_x(f_n)|^2}{\sum_n PWF(f_n)}}$$

Channel Signal-to-Noise Ratio (SNR)

$$SNR_{pwr} = 20 \cdot \log \left(\frac{10^{\frac{ILfit(f_{NQ})}{20}}}{\sigma_{xtp} + \sigma_{ILN}} \right)$$

Insertion loss and crosstalk deviations are measures of noise caused by channel reflections and crosstalk

Channel Quality Metrics



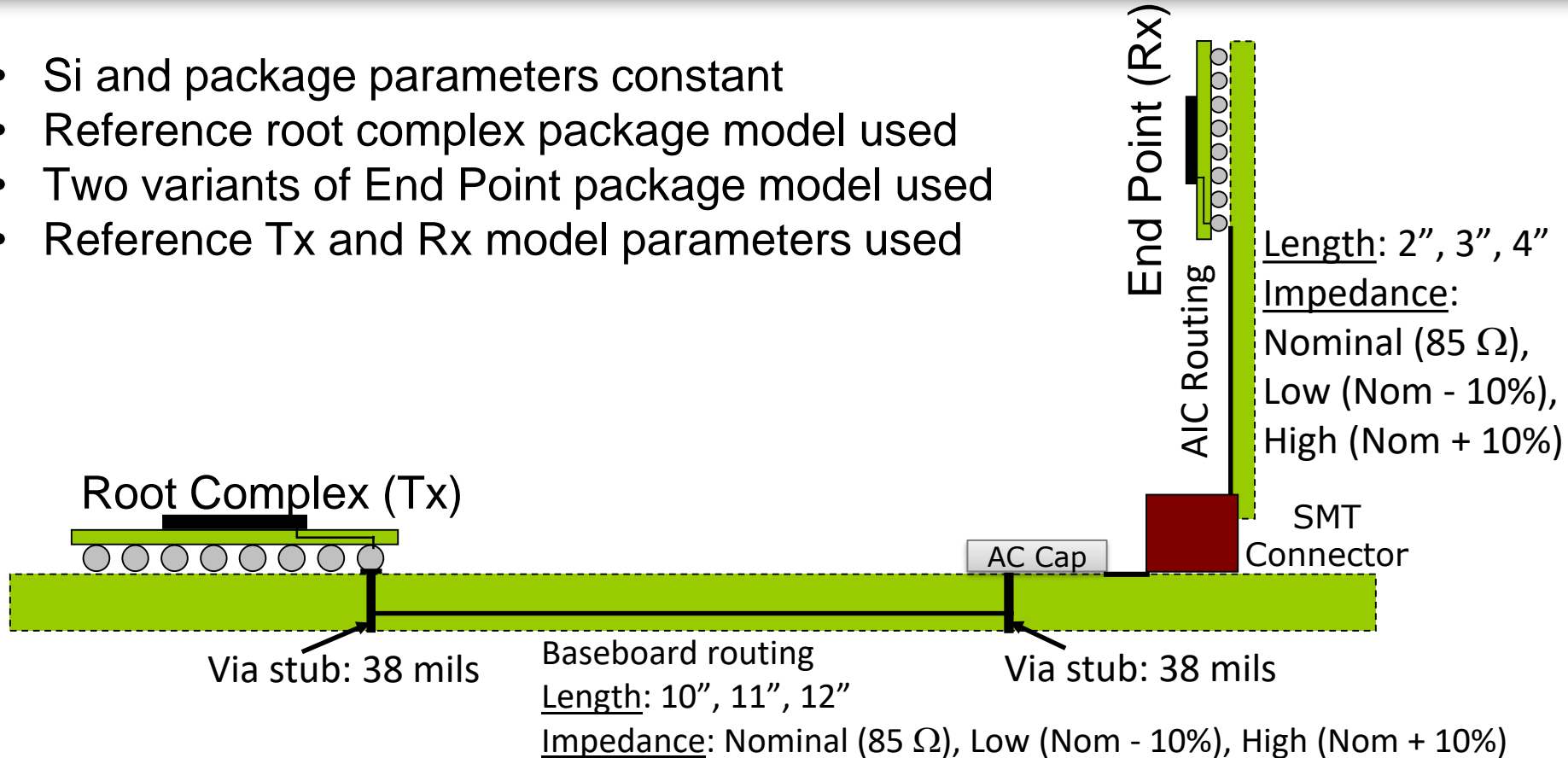
Fitted Insertion Loss (IL_FIT) at 16 GHz	-33.7 dB
Insertion Loss Noise (iln)	8.56 mV
Crosstalk Noise (icn)	5.17 mV
Channel Signal-to-Noise Ratio (SNR)	19.6 dB

Channel with SNR ~ 20 dB is a good quality channel at 32GT/s

Impact of Channel Design and Manufacturing Variations

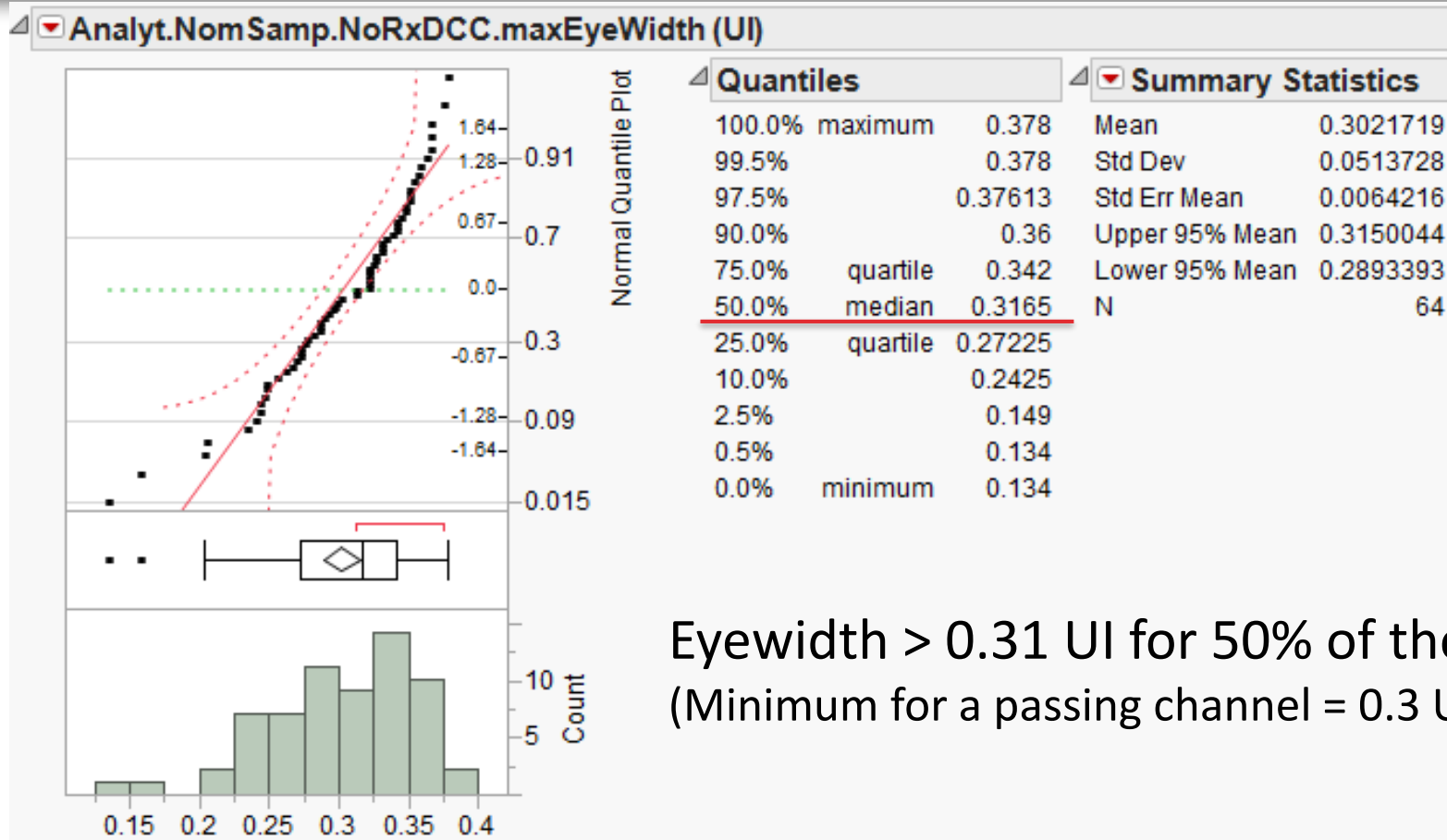
Channel Variation: 1 Conn Topology

- Si and package parameters constant
- Reference root complex package model used
- Two variants of End Point package model used
- Reference Tx and Rx model parameters used



Routing Lengths and Impedances are key variables

Impact of Variation on Eyewidth

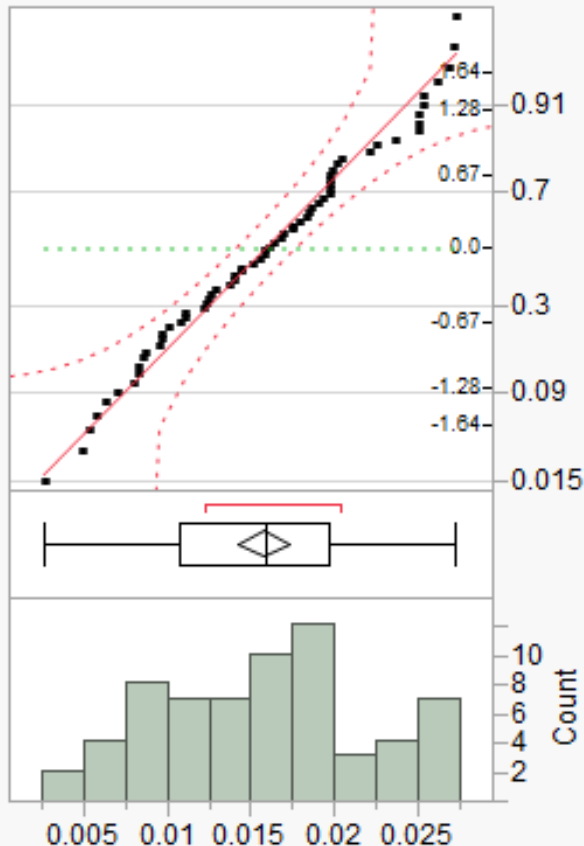


Eyewidth > 0.31 UI for 50% of the cases
(Minimum for a passing channel = 0.3 UI)

Length & impedance variations make eyewidth vary by > 20% UI

Impact of Variation on Eyeheight

▼ Analyt.NomSamp.NoRxDCC.maxEyeHeight (V)



Quantiles

100.0%	maximum	0.0272
99.5%		0.0272
97.5%		0.02708
90.0%		0.0251
75.0%	quartile	0.0197
50.0%	median	0.0159
25.0%	quartile	0.01078
10.0%		0.00747
2.5%		0.00402
0.5%		0.00263
0.0%	minimum	0.00263

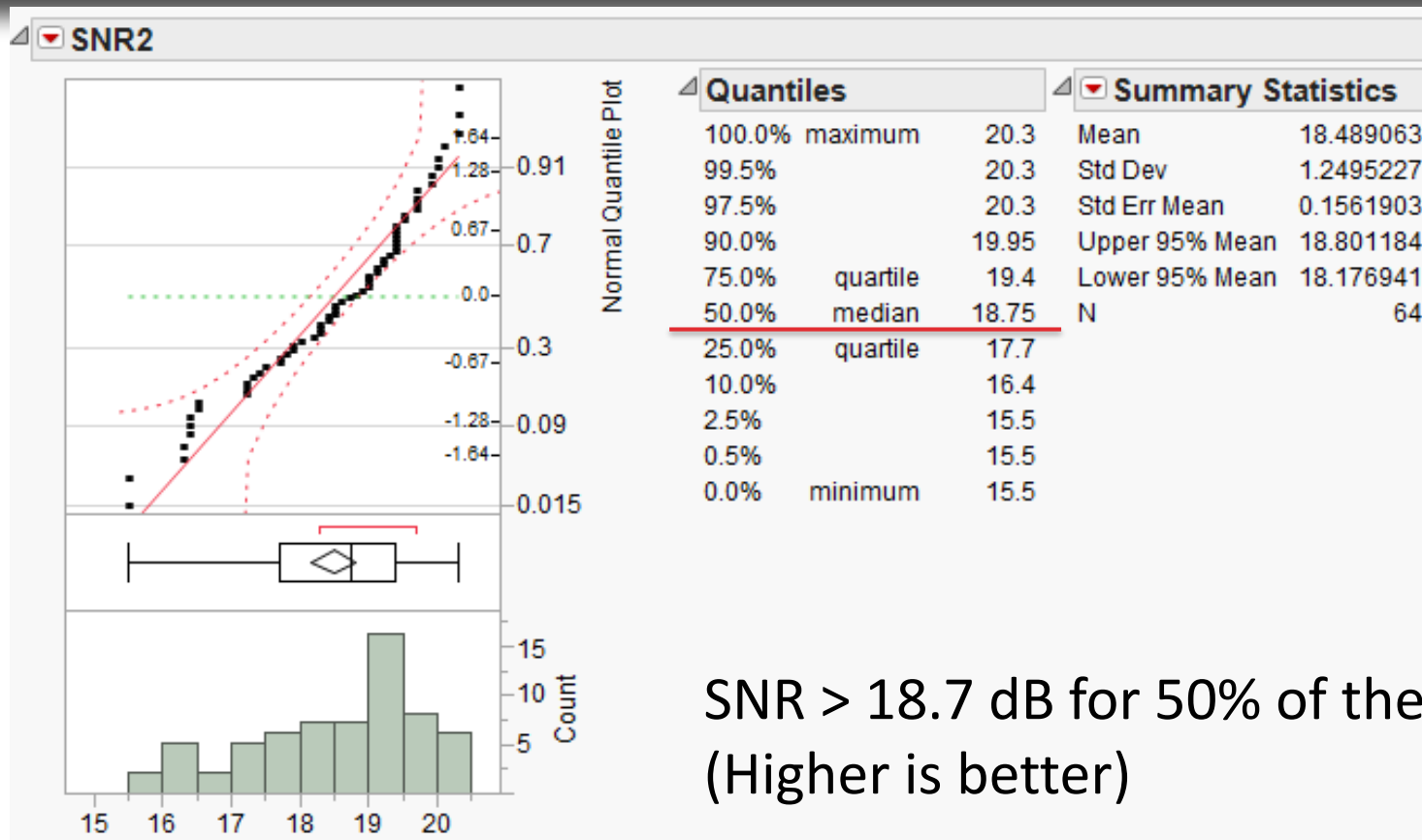
Summary Statistics

Mean	0.0157911
Std Dev	0.0062737
Std Err Mean	0.0007842
Upper 95% Mean	0.0173582
Lower 95% Mean	0.014224
N	64

Eyeheight > 15 mV for 50% of the cases
(Minimum for a passing channel = 10 mV)

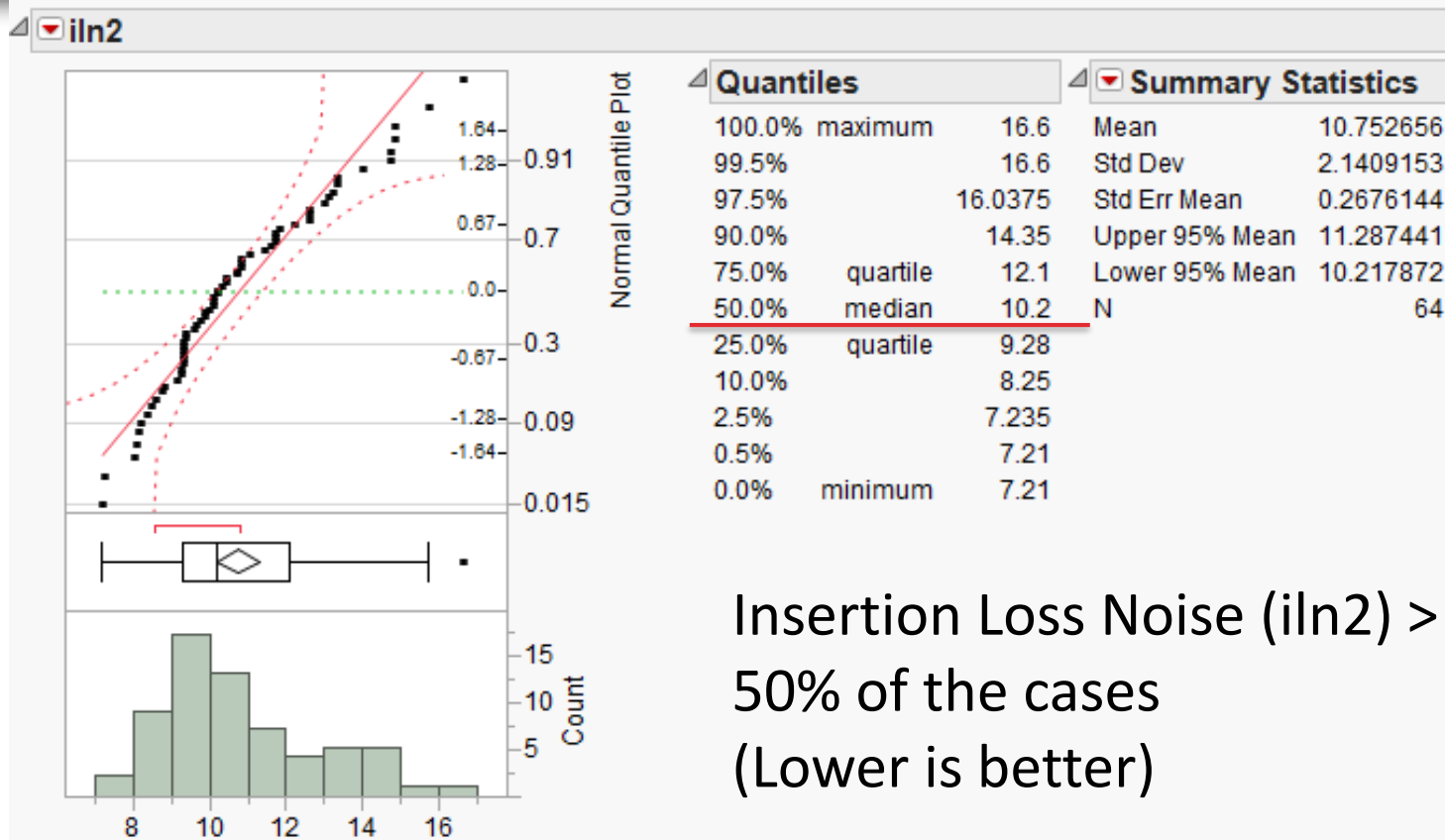
Length & impedance variations make eyeheight vary by > 5x

Impact of Variation on Signal-to-Noise Ratio



Length & impedance variations make Signal-to-Noise ratio vary by ~ 5 dB

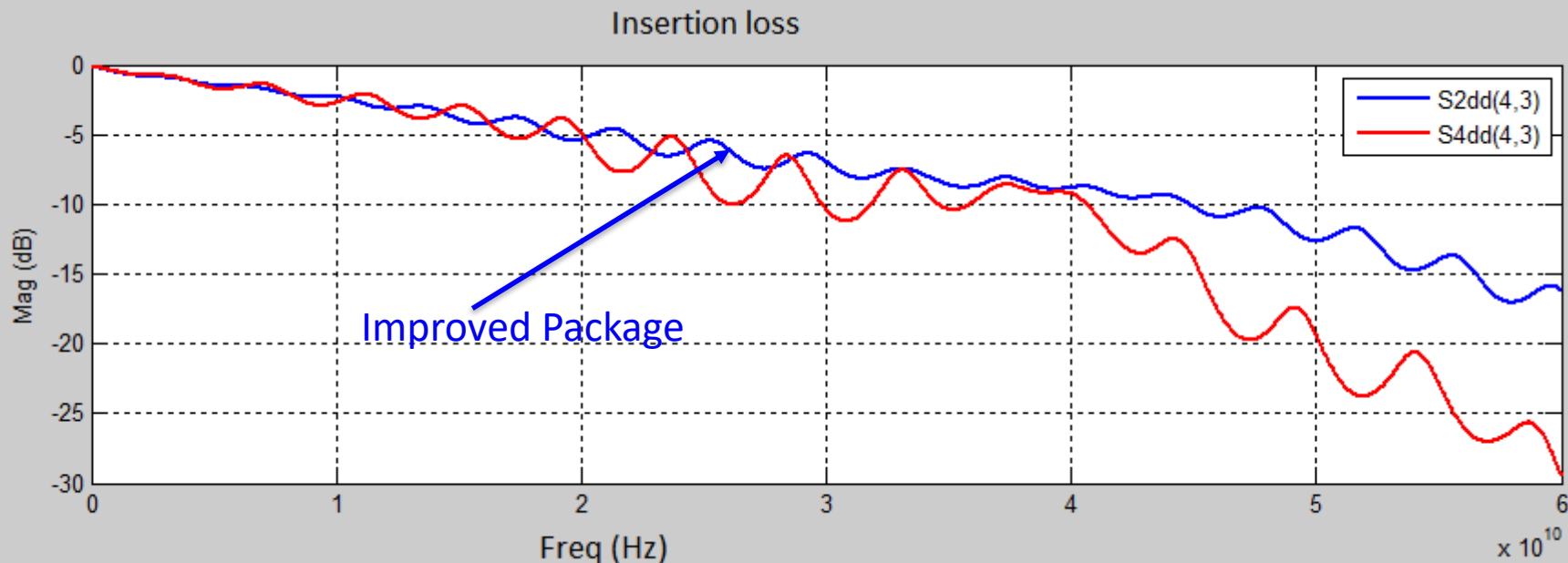
Impact of Variation on Insertion Loss Noise



Insertion Loss Noise (iln2) > 10 mV for 50% of the cases
(Lower is better)

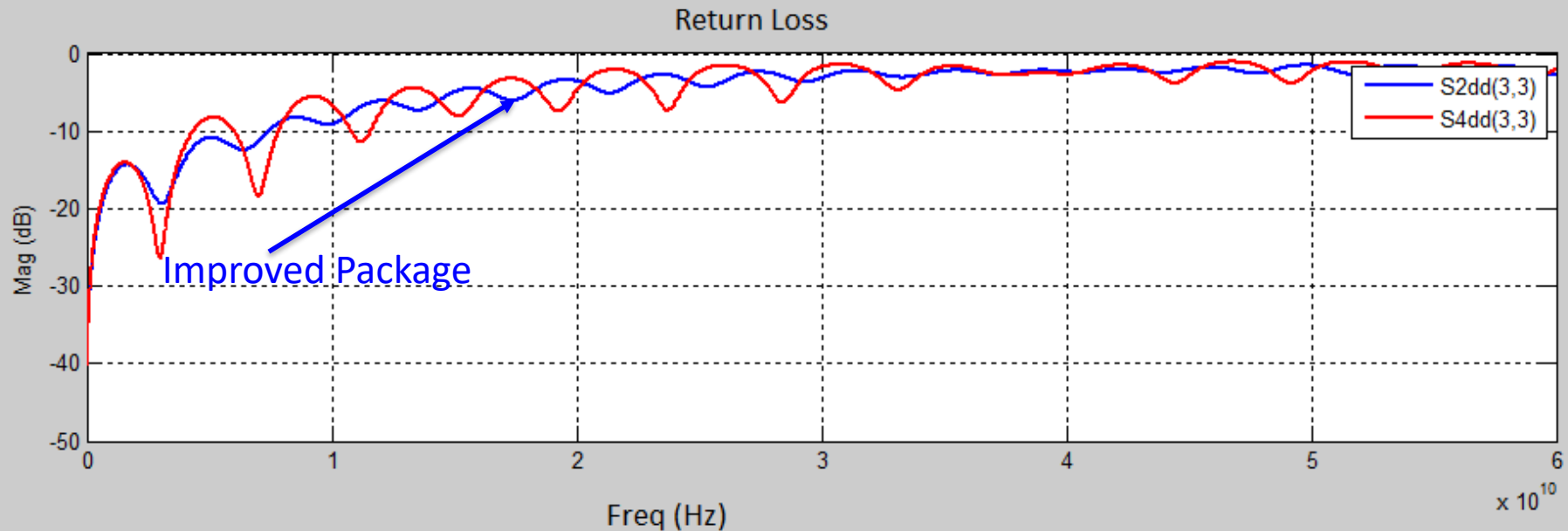
Length & impedance variations make reflection-induced insertion loss noise (iln2) vary by > 2x

End Point Package Improvement



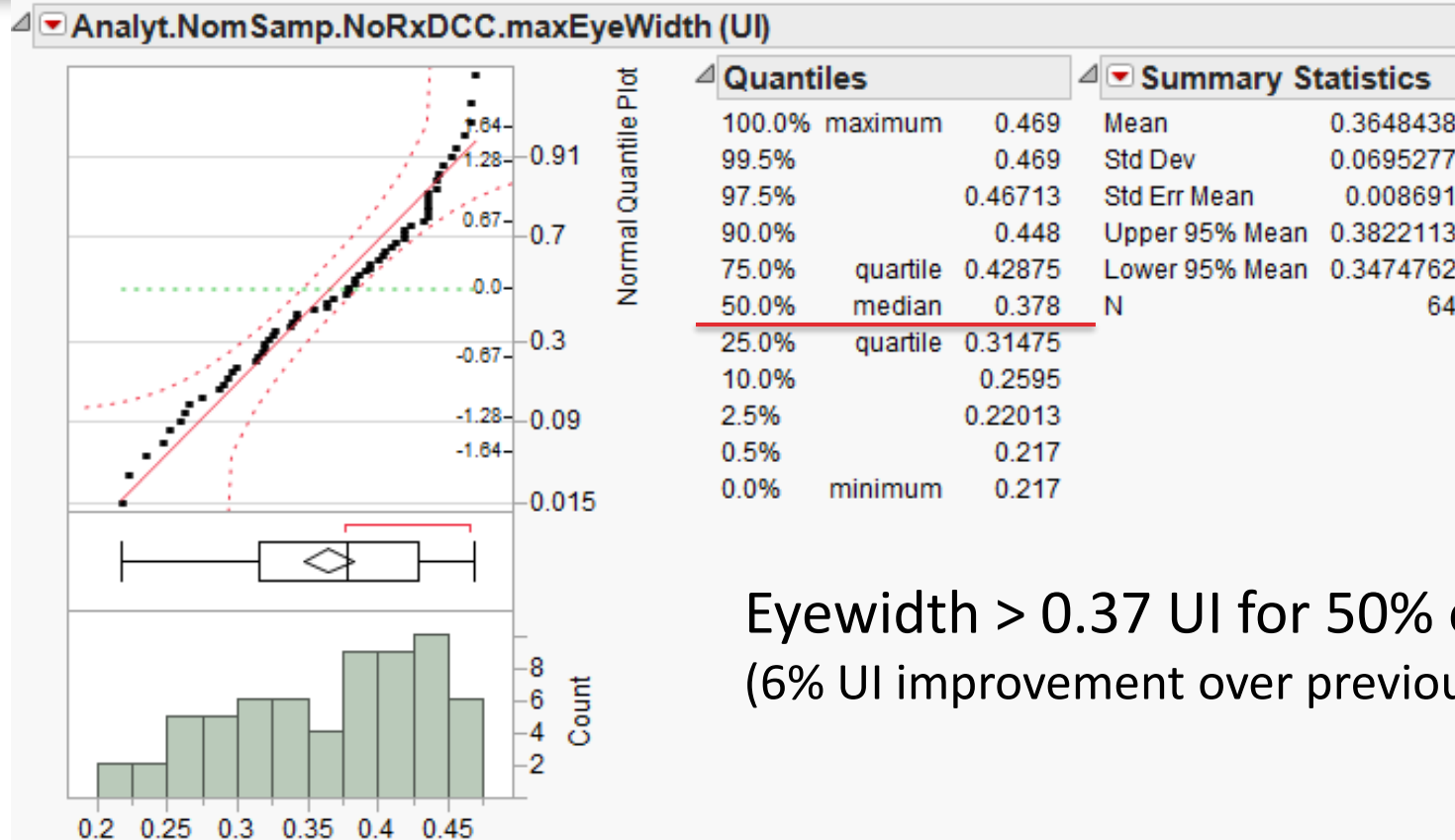
End Point package was improved by reducing the capacitive discontinuity at the BGA interface

End Point Package Improvement



End Point package optimization leads to return loss improvement

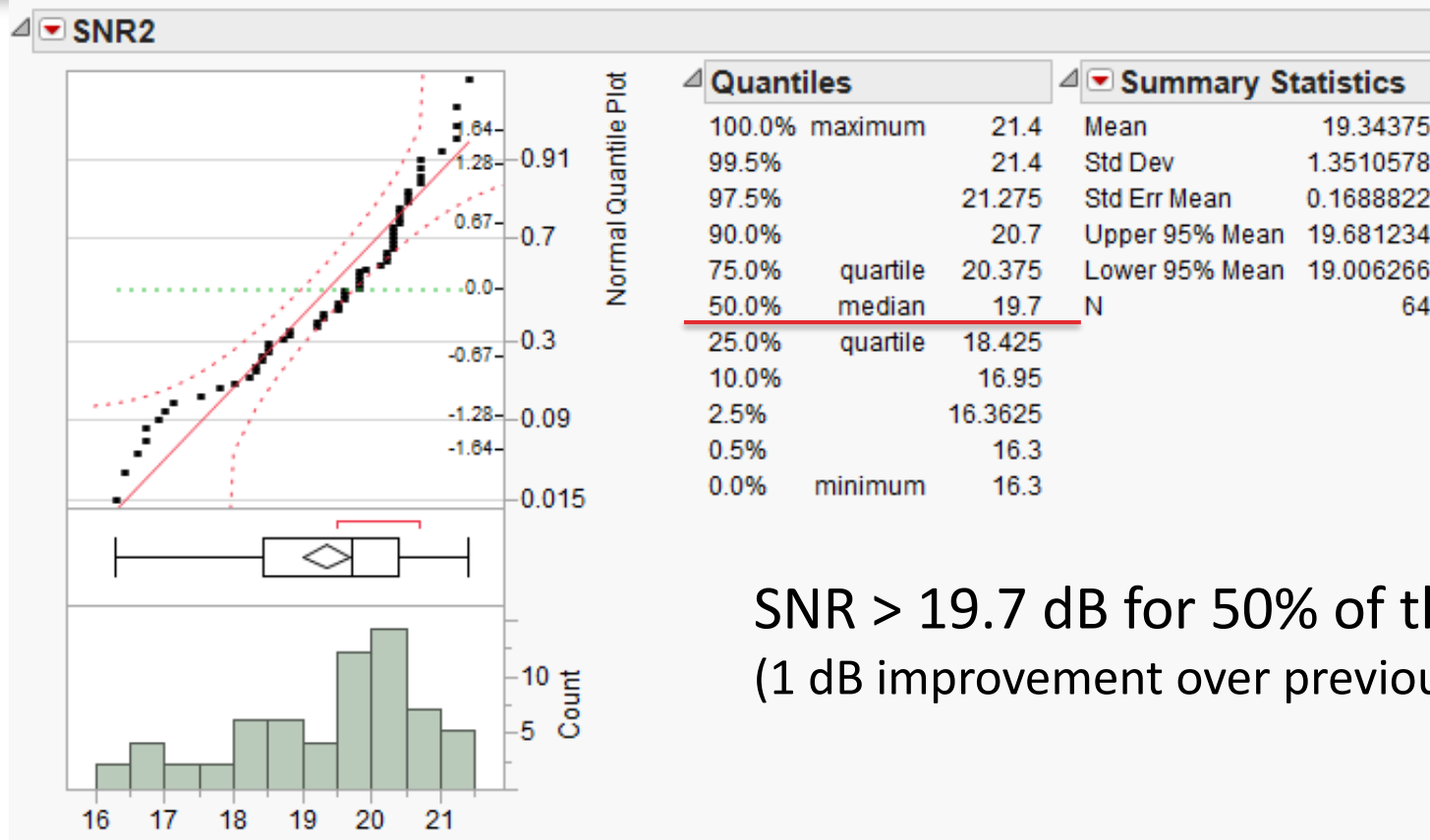
Impact of End Point Package Improvement on Eyewidth



Eyewidth > 0.37 UI for 50% of the cases
(6% UI improvement over previous package)

End Point package improvement makes ~25% more cases to
pass $EW \geq 0.3$ UI

Impact of End Point Package Improvement on Signal-to-Noise Ratio

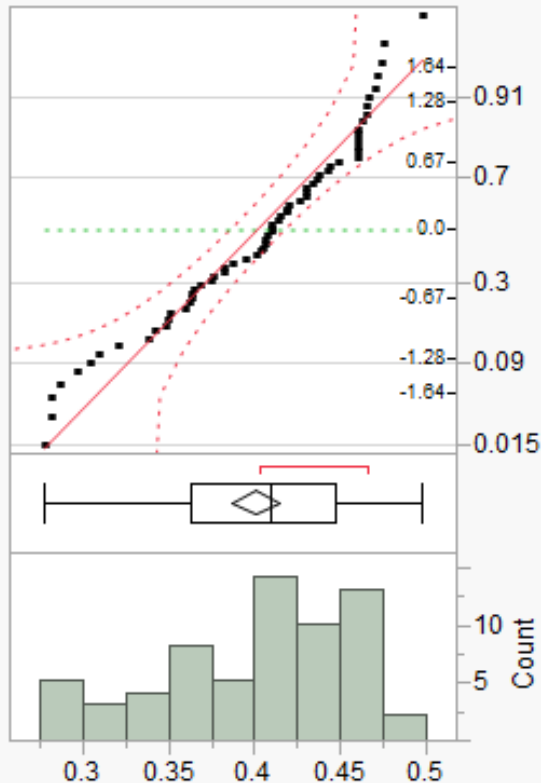


SNR > 19.7 dB for 50% of the cases
(1 dB improvement over previous package)

1 dB channel SNR improvement expands the solution space by
~25%

Impact of End Point Package and Via Stub Improvement on Eyewidth

▼ Analyt.NomSamp.NoRxDCC.maxEyeWidth (UI)



Quantiles

100.0%	maximum	0.497
99.5%		0.497
97.5%		0.48325
90.0%		0.4655
75.0%	quartile	0.44675
50.0%	median	0.409
25.0%	quartile	0.363
10.0%		0.3065
2.5%		0.2805
0.5%		0.278
0.0%	minimum	0.278

Summary Statistics

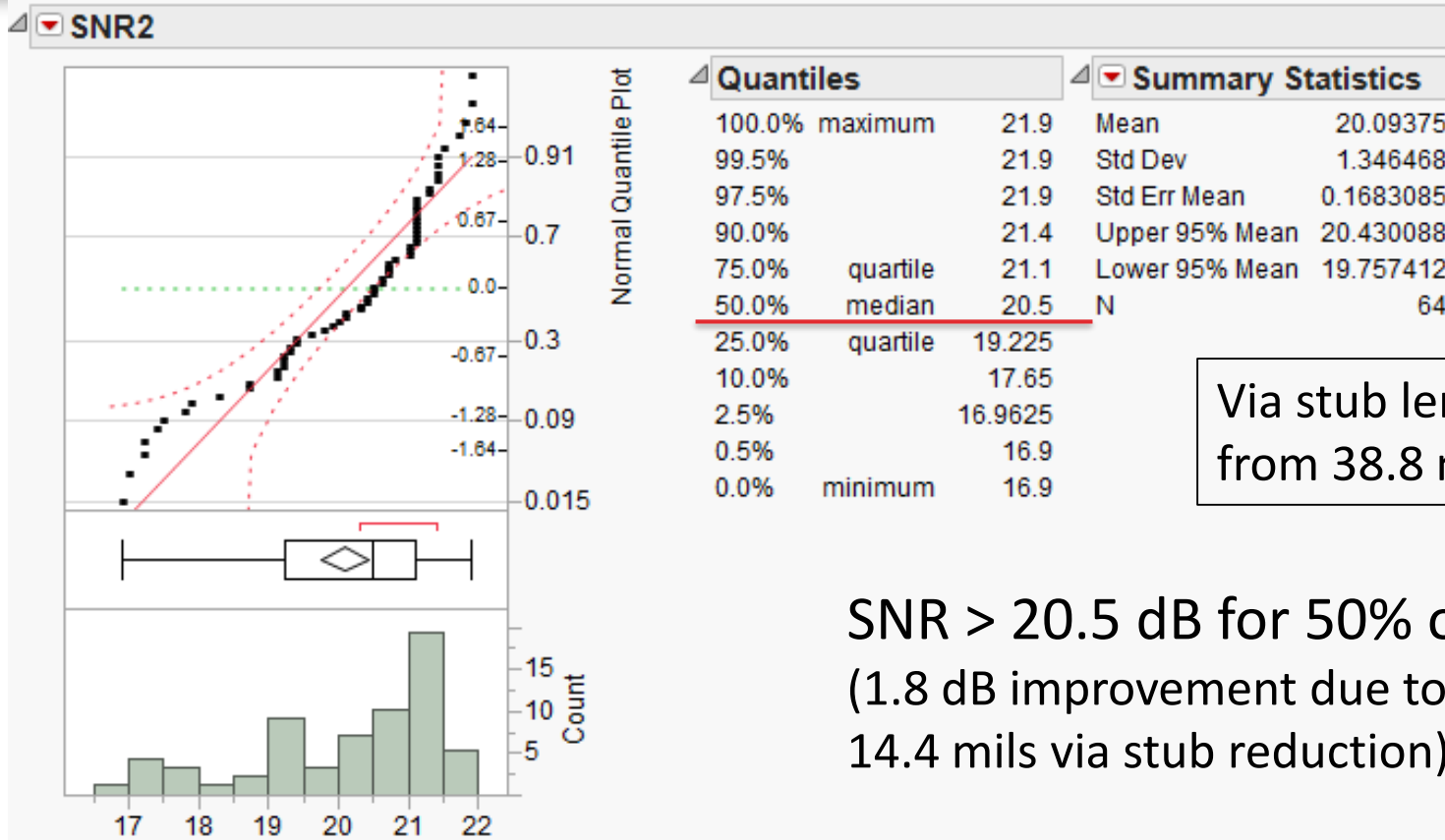
Mean	0.400875
Std Dev	0.0560973
Std Err Mean	0.0070122
Upper 95% Mean	0.4148877
Lower 95% Mean	0.3868623
N	64

Via stub length reduced
from 38.8 mils to 24.4 mils

Eyewidth > 0.4 UI for 50% of the cases
(10% UI improvement due to package and
14.4 mils via stub reduction)

End Point package improvement and 14.4 mils via stub
reduction expand the channel solution space by ~35%

Impact of End Point Package and Via Stub Improvement on SNR



1.8 dB channel SNR improvement expands the channel solution space by ~35%

Summary



- Meg6-like (~ 1 dB/in at 16 GHz) PCB material is necessary for 12"+ baseboard routing
- Via stub length < 25 mils is a significant enabler
- PCB impedance variation should be controlled within $\pm 10\%$
- Package should be optimized to minimize return loss better than -6 dB up to 16 GHz
- The difference between pad-to-pad insertion loss and FEXT should be > 20 dB from low frequency to 16 GHz
- NEXT should be minimized below -65 dB from DC to 16 GHz
- Channel metrics are useful indicators of the channel quality
- Pre-Si channel compliance simulations across HVM conditions are necessary for 32GT/s channel design

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